

## CLAIMS

What is claimed is:

- 1    1.    An apparatus, comprising:  
2        an interrupt cause register;  
3        an interrupt disabling register capable of being operatively coupled to the  
4 interrupt cause register; and  
5        an interrupt mask register capable of being operatively coupled to the  
6 interrupt disabling register.
- 1    2.    The apparatus of claim 1, wherein the interrupt cause register, the interrupt  
2 disabling register, and the interrupt mask register are included in a single monolithic  
3 memory circuit.
- 1    3.    The apparatus of claim 1, wherein the interrupt cause register, the interrupt  
2 disabling register, and the interrupt mask register are included in a single  
3 programmable interrupt controller.
- 1    4.    The apparatus of claim 1, further comprising:  
2        an arithmetic logic unit capable of being operatively coupled to the interrupt  
3 mask register.
- 1    5.    The apparatus of claim 1, further comprising:  
2        an interrupt disabling override register capable of being operatively coupled  
3 to the interrupt mask register.
- 1    6.    The apparatus of claim 1, further comprising:  
2        a device driver capable of being operatively coupled to the interrupt  
3 disabling register.

1 7. A system, comprising:  
2 a processor;  
3 a bus capable of being operatively coupled to the processor;  
4 an interrupt cause register capable of being operatively coupled to the bus;  
5 an interrupt disabling register capable of being operatively coupled to the  
6 interrupt cause register; and  
7 an interrupt mask register capable of being operatively coupled to the  
8 interrupt disabling register.

1 8. The system of claim 7, further comprising:  
2 a device capable of generating an interrupt and capable of being operatively  
3 coupled to the bus.

1 9. The system of claim 8, wherein the device is a network adapter.

1 10. The system of claim 8, wherein the device is a graphics display controller.

1 11. The system of claim 8, wherein the device is a storage device.

1 12. The system of claim 7, wherein the bus is a Peripheral Component  
2 Interconnect (PCI) bus.

1 13. The system of claim 7, wherein reading the interrupt cause register in  
2 response to an interrupt generated by a device operatively coupled to the processor  
3 results in transferring a value stored in the interrupt disabling register to the  
4 interrupt mask register.

1 14. The system of claim 7, further comprising:  
2 a memory capable of being operatively coupled to the processor, the  
3 memory being used to store a set of program instructions comprising a portion of an  
4 interrupt service routine.

1 15. A method, comprising:  
2 reading an interrupt cause register in response to receiving an interrupt;  
3 transferring a value stored in an interrupt disabling register corresponding to  
4 a source of the interrupt to an interrupt mask register so as to disable receiving  
5 further interrupts from the source of the interrupt.

1 16. The method of claim 15, further comprising:  
2 generating the interrupt.

1 17. The method of claim 15, further comprising:  
2 executing an interrupt service routine to acknowledge the interrupt

1 18. The method of claim 15, further comprising:  
2 writing an override value to an interrupt disabling override register; and  
3 transferring the override value to the interrupt mask register so as to enable  
4 receiving further interrupts from the source of the interrupt.

1 19. An article comprising a machine-accessible medium having associated data,  
2 wherein the data, when accessed, results in a machine performing:  
3 reading an interrupt cause register in response to receiving an interrupt;  
4 transferring a value stored in an interrupt disabling register corresponding to  
5 a source of the interrupt to an interrupt mask register so as to disable receiving  
6 further interrupts from the source of the interrupt.

1 20. The article of claim 19, wherein the machine-accessible medium further  
2 includes data, which when accessed by the machine, results in the machine  
3 performing:  
4 writing a message signaling interrupt message to a memory location.

1 21. The article of claim 19, wherein transferring a value stored in an interrupt  
2 disabling register corresponding to a source of the interrupt to an interrupt mask  
3 register includes:  
4 refraining from accessing a bus capable of being operatively coupled to the  
5 source of the interrupt and the interrupt cause register.

1 22. The article of claim 19, wherein the machine-accessible medium further  
2 includes data, which when accessed by the machine, results in the machine  
3 performing:  
4 generating a multiplicity of interrupts using the source of the interrupt;  
5 repeatedly reading the interrupt cause register in response to receiving the  
6 multiplicity of interrupts; and  
7 repeatedly transferring the value stored in the interrupt disabling register  
8 corresponding to the source of the interrupt to the interrupt mask register.